

### In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 10. (Canceled)

1        11. (New) A 4-bit carry look ahead circuit forming a  
2 combined propagate signal and a combined generated signal  
3 comprising:

4        a first NAND gate (101) having a first input receiving a  
5 propagate signal from a first bit, a second input receiving a  
6 propagate signal from the second bit and an output;

7        a second NAND gate (102) having a first input receiving a  
8 propagate signal from the third bit, a second input receiving a  
9 propagate signal from the fourth bit and an output;

10       a NOR gate (103) having a first input connected to said  
11 output of said first NAND gate, a second input connected to said  
12 output of said second NAND gate and an output forming the  
13 combined propagate signal for the four bits;

14       a first AND-NOR gate (201) having a first AND input  
15 receiving a generate signal from the first bit, a second AND  
16 input receiving a propagate signal from the second bit, a NOR  
17 input receiving a generate signal from the second bit and an  
18 output;

19       a second AND-NOR gate (202) having a first AND input  
20 receiving a generate signal from the third bit, a second AND  
21 input receiving a propagate signal from the fourth bit, a NOR  
22 input receiving a generate signal from the fourth bit and an  
23 output; and

24       a OR-NAND gate (251) having a first OR input connected to  
25 said output of said first AND-NOR gate, a second OR input  
26 connected to said output of said second NAND gate, a NAND input

27 connected to said output of said second AND-NOR gate and an  
28 output forming the combined generate signal for the four bits.

1 12. (New) The carry look ahead circuit of claim 11, wherein:  
2 said first and second AND-NOR gates include  
3 a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said first AND input,  
6 a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and a gate connected to said second AND  
9 input,  
10 a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and the  
12 output and a gate connected to said NOR input,  
13 a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,  
16 a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and  
19 a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1 13. (New) The carry look ahead circuit of claim 11, wherein:  
2 said first and second AND-NOR gates include  
3 a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said NOR input,  
6 a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first

8 intermediate node and said output and a gate connected to  
9 said first AND input,

10 a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and said  
12 output and a gate connected to said second AND input,

13 a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16 a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19 a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1 14. (New) The carry look ahead circuit of claim 11, wherein:  
2 said OR-NAND gate includes

3 a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6 a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9 a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12 a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said OR input,

15 a second N-channel transistor having a source-drain  
16 path connected between said second intermediate node and  
17 ground and a gate connected to said first OR input, and

18           a third N-channel transistor having a source-drain path  
19 connected between said second intermediate node and ground  
20 and a gate connected to said second OR input.

1       15. (New) The carry look ahead circuit of claim 11, wherein:  
2       said OR-NAND gate includes  
3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,  
6           a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,  
9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,  
12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said first OR input,  
15           a second N-channel transistor having a source-drain  
16 path connected between said output and said second  
17 intermediate node and a gate connected to said second OR  
18 input, and  
19           a third N-channel transistor having a source-drain path  
20 connected between said second intermediate node and ground  
21 and a gate connected to said NAND input.

1       16. (New) A 5-bit carry look ahead circuit forming a  
2 combined propagate signal and a combined generated signal  
3 comprising:  
4           a first NAND gate (104) having a first input receiving a  
5 propagate signal from the first bit, a second input receiving a  
6 propagate signal from the second bit and an output;

7        a second NAND gate (105) having a first input receiving a  
8 propagate signal from the third bit, a second input receiving a  
9 propagate signal from the fourth bit and an output;  
10       a first NOR gate (106) having a first input connected to  
11 said output of said first NAND gate, a second input connected to  
12 said output of said second NAND gate and an output;  
13       a second NOR gate (107) having a first input connected to  
14 said output of said first NOR gate, a second input receiving a  
15 propagate signal from the fifth bit and an output;  
16       a first inverter (301) having a input connected to said  
17 output of said second NOR gate and an output generating the  
18 combined propagate signal for the five bits;  
19       a first AND-NOR gate (203) having a first AND input  
20 receiving a generate signal from the first bit, a second AND  
21 input receiving a propagate signal from the second bit, a NOR  
22 input receiving a generate signal from the second bit and an  
23 output;  
24       a second AND-NOR gate (204) having a first AND input  
25 receiving a generate signal from the third bit, a second AND  
26 input receiving a propagate signal from the fourth bit, a NOR  
27 input receiving a generate signal from the fourth bit and an  
28 output;  
29       a OR-NAND gate (252) having a first OR input connected to  
30 said output of said first AND-NOR gate, a second OR input  
31 connected to said output of said second NAND gate, a NAND input  
32 connected to said output of said second AND-NOR gate and an  
33 output forming the combined generate signal for the four bits;  
34       a third AND-NOR gate (205) having a first AND input  
35 connected to said output of said OR-NAND gate, a second AND input  
36 receiving a propagate signal from the fifth bit, a NOR input  
37 receiving a generate signal from the fifth bit and an output; and

38        a second inverter (302) having an input connected to said  
39        output of said third AND-NOR gate and an output generating the  
40        combined generate signal for the five bits.

1        17. (New) The carry look ahead circuit of claim 16, wherein:  
2        said first, second and third AND-NOR gates include  
3                a first P-channel transistor having a source-drain path  
4        connected between a supply voltage and an first intermediate  
5        node and a gate connected to said first AND input,  
6                a second P-channel transistor having a source-drain  
7        path connected between a supply voltage and said first  
8        intermediate node and a gate connected to said second AND  
9        input,  
10               a third P-channel transistor having a source-drain path  
11        connected between said first intermediate node and the  
12        output and a gate connected to said NOR input,  
13               a first N-channel transistor having a source-drain path  
14        connected between said output and a second intermediate node  
15        and a gate connected to said first AND input,  
16               a second N-channel transistor having a source-drain  
17        path connected between said second intermediate node and  
18        ground and a gate connected to said second AND input, and  
19               a third N-channel transistor having a source-drain path  
20        connected between said output and ground and a gate  
21        connected to said NOR input.

1        18. (New) The carry look ahead circuit of claim 16, wherein:  
2        said first, second and third AND-NOR gates include  
3                a first P-channel transistor having a source-drain path  
4        connected between a supply voltage and an first intermediate  
5        node and a gate connected to said NOR input,

6           a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and said output and a gate connected to  
9 said first AND input,

10          a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and said  
12 output and a gate connected to said second AND input,

13          a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16          a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19          a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1       19. (New) The carry look ahead circuit of claim 16, wherein:  
2 said OR-NAND gate includes

3          a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6          a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9          a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12          a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said OR input,

15           a second N-channel transistor having a source-drain  
16 path connected between said second intermediate node and  
17 ground and a gate connected to said first OR input, and  
18           a third N-channel transistor having a source-drain path  
19 connected between said second intermediate node and ground  
20 and a gate connected to said second OR input.

1       20. (New) The carry look ahead circuit of claim 16, wherein:  
2       said OR-NAND gate includes  
3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,  
6           a first N-channel transistor having a source-drain path  
7 connected between said output and a second intermediate node  
8 and a gate connected to said first OR input,  
9           a second P-channel transistor having a source-drain  
10 path connected between said first intermediate node and said  
11 output and a gate connected to said first OR input,  
12           a third P-channel transistor having a source-drain path  
13 connected between the supply voltage and said output and a  
14 gate connected to said NAND input,  
15           a second N-channel transistor having a source-drain  
16 path connected between said output and said second  
17 intermediate node and a gate connected to said second OR  
18 input, and  
19           a third N-channel transistor having a source-drain path  
20 connected between said second intermediate node and ground  
21 and a gate connected to said NAND input.

1       21. (New) A 5-bit carry look ahead circuit forming a  
2 combined propagate signal and a combined generated signal  
3 comprising:



4       a first NAND gate (108) having a first input receiving a  
5 propagate signal from the first bit, a second input receiving a  
6 propagate signal from the second bit and an output;  
7       a second NAND gate (109) having a first input receiving a  
8 propagate signal from the third bit, a second input receiving a  
9 propagate signal from the fourth bit and an output;  
10       a first inverter (303) having an input connected to said  
11 output of said second NAND gate and an output;  
12       a third NAND gate (119) having a first input connected to  
13 said output of said first inverter, a second input receiving a  
14 propagate signal from the fifth bit and an output;  
15       a NOR gate (111) having a first input connected to said  
16 output of said first NAND gate, a second input connected to said  
17 output of said third NAND gate and an output generating the  
18 combined propagate signal for the five bits;  
19       a first AND-NOR gate (206) having a first AND input  
20 receiving a generate signal from the first bit, a second AND  
21 input receiving a propagate signal from the second bit, a NOR  
22 input receiving a generate signal from the second bit and an  
23 output;  
24       a second AND-NOR (207) gate having a first AND input  
25 receiving a generate signal from the third bit, a second AND  
26 input receiving a propagate signal from the fourth bit, a NOR  
27 input receiving a generate signal from the fourth bit and an  
28 output;  
29       a second inverter (304) having an input connected to said  
30 output of said second AND-NOR gate and an output;  
31       a third AND-NOR gate (208) having a first AND input  
32 connected to said output of said second inverter, a second AND  
33 input receiving a propagate signal from the fifth bit, a NOR  
34 input receiving a generate signal from the fifth bit and an  
35 output; and

36       a OR-NAND gate (253) having a first OR input connected to  
37 said output of said first AND-NOR gate, a second OR input  
38 connected to said output of said third AND-NOR gate, a NAND input  
39 connected to said output of said third AND-NOR gate and an output  
40 forming the combined generate signal for the four bits.

1       22. (New) The carry look ahead circuit of claim 21, wherein:  
2       said first, second and third AND-NOR gates include  
3       a first P-channel transistor having a source-drain path  
4       connected between a supply voltage and an first intermediate  
5       node and a gate connected to said first AND input,  
6       a second P-channel transistor having a source-drain  
7       path connected between a supply voltage and said first  
8       intermediate node and a gate connected to said second AND  
9       input,  
10       a third P-channel transistor having a source-drain path  
11       connected between said first intermediate node and the  
12       output and a gate connected to said NOR input,  
13       a first N-channel transistor having a source-drain path  
14       connected between said output and a second intermediate node  
15       and a gate connected to said first AND input,  
16       a second N-channel transistor having a source-drain  
17       path connected between said second intermediate node and  
18       ground and a gate connected to said second AND input, and  
19       a third N-channel transistor having a source-drain path  
20       connected between said output and ground and a gate  
21       connected to said NOR input.

1       23. (New) The carry look ahead circuit of claim 21, wherein:  
2       said first, second and third AND-NOR gates include

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said NOR input,

6           a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and said output and a gate connected to  
9 said first AND input,

10          a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and said  
12 output and a gate connected to said second AND input,

13          a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16          a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19          a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1       24. (New) The carry look ahead circuit of claim 21, wherein:  
2 said OR-NAND gate includes

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6           a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said OR input,

15           a second N-channel transistor having a source-drain  
16 path connected between said second intermediate node and  
17 ground and a gate connected to said first OR input, and

18           a third N-channel transistor having a source-drain path  
19 connected between said second intermediate node and ground  
20 and a gate connected to said second OR input.

1       25. (New) The carry look ahead circuit of claim 21, wherein:  
2 said OR-NAND gate includes

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6           a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said first OR input,

15           a second N-channel transistor having a source-drain  
16 path connected between said output and said second  
17 intermediate node and a gate connected to said second OR  
18 input, and

19           a third N-channel transistor having a source-drain path  
20 connected between said second intermediate node and ground  
21 and a gate connected to said NAND input.

1        26. (New) A 5-bit carry look ahead circuit forming a  
2 combined propagate signal and a combined generated signal  
3 comprising:  
4        a first NAND gate (112) having a first input receiving a  
5 propagate signal from the second bit, a second input receiving a  
6 propagate signal from the third bit and an output;  
7        a second NAND gate (113) having a first input receiving a  
8 propagate signal from the fourth bit, a second input receiving a  
9 propagate signal from the fifth bit and an output;  
10       a NOR gate (114) having a first input connected to said  
11 output of said first NAND gate, a second input connected to said  
12 output of said second NAND gate and an output;  
13       a third NAND gate (115) having a first input receiving the  
14 propagate signal from the first bit, a second input connected to  
15 said output of said NOR gate and an output;  
16       a first inverter (305) having an input connected to said  
17 output of said third NAND gate and an output generating the  
18 combined propagate signal for the five bits;  
19       a first AND-NOR gate (209) having a first AND input  
20 receiving a propagate signal from the third bit, a second AND  
21 input receiving a generate signal from the second bit, a NOR  
22 input receiving a generate signal from the third bit and an  
23 output;  
24       a second AND-NOR (210) gate having a first AND input  
25 receiving a propagate signal from the fifth bit, a second AND  
26 input receiving a generate signal from the fourth bit, a NOR  
27 input receiving a generate signal from the fifth bit and an  
28 output;  
29       a OR-NAND gate (254) having a first OR input connected to  
30 said output of said first AND-NOR gate, a second OR input  
31 connected to said output of said second NAND gate, a NAND input

32 connected to said output of said first AND-NOR gate and an  
33 output;

34 a third AND-NOR gate (211) having a first AND input  
35 connected to said output of said NOR gate, a second AND input  
36 receiving a generate signal from the first bit, a NOR input  
37 connected to said output of said OR-NAND gate and an output; and

38 a second inverter (306) having an input connected to said  
39 output of said third AND-NOR gate and an output generation the  
40 combined generate signal for the five bits.

1 27. (New) The carry look ahead circuit of claim 26, wherein:  
2 said first, second and third AND-NOR gates include

3 a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said first AND input,

6 a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and a gate connected to said second AND  
9 input,

10 a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and the  
12 output and a gate connected to said NOR input,

13 a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16 a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19 a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1       28. (New) The carry look ahead circuit of claim 26, wherein:  
2       said first, second and third AND-NOR gates include

3           a first P-channel transistor having a source-drain path  
4       connected between a supply voltage and an first intermediate  
5       node and a gate connected to said NOR input,

6           a second P-channel transistor having a source-drain  
7       path connected between a supply voltage and said first  
8       intermediate node and said output and a gate connected to  
9       said first AND input,

10          a third P-channel transistor having a source-drain path  
11       connected between said first intermediate node and said  
12       output and a gate connected to said second AND input,

13          a first N-channel transistor having a source-drain path  
14       connected between said output and a second intermediate node  
15       and a gate connected to said first AND input,

16          a second N-channel transistor having a source-drain  
17       path connected between said second intermediate node and  
18       ground and a gate connected to said second AND input, and

19          a third N-channel transistor having a source-drain path  
20       connected between said output and ground and a gate  
21       connected to said NOR input.

1       29. (New) The carry look ahead circuit of claim 26, wherein:  
2       said OR-NAND gate includes

3           a first P-channel transistor having a source-drain path  
4       connected between a supply voltage and an first intermediate  
5       node and a gate connected to said second OR input,

6           a second P-channel transistor having a source-drain  
7       path connected between said first intermediate node and said  
8       output and a gate connected to said first OR input,

9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said OR input,

15           a second N-channel transistor having a source-drain  
16 path connected between said second intermediate node and  
17 ground and a gate connected to said first OR input, and

18           a third N-channel transistor having a source-drain path  
19 connected between said second intermediate node and ground  
20 and a gate connected to said second OR input.

1       30. (New) The carry look ahead circuit of claim 26, wherein:  
2 said OR-NAND gate includes

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6           a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said first OR input,

15           a second N-channel transistor having a source-drain  
16 path connected between said output and said second  
17 intermediate node and a gate connected to said second OR  
18 input, and



19           a third N-channel transistor having a source-drain path  
20       connected between said second intermediate node and ground  
21       and a gate connected to said NAND input.

1       31. (New) A 5-bit carry look ahead circuit forming a  
2       combined propagate signal and a combined generated signal  
3       comprising:

4       a first NAND gate (116) having a first input receiving a  
5       propagate signal from the second bit, a second input receiving a  
6       propagate signal from the third bit and an output;

7       a second NAND gate (117) having a first input receiving a  
8       propagate signal from the fourth bit, a second input receiving a  
9       propagate signal from the fifth bit and an output;

10       a NOR gate (118) having a first input connected to said  
11       output of said first NAND gate, a second input connected to said  
12       output of said second NAND gate and an output;

13       a third NAND gate (119) having a first input receiving the  
14       propagate signal from the first bit, a second input connected to  
15       said output of said NOR gate and an output;

16       a first inverter (310) having an input connected to said  
17       output of said third NAND gate and an output generating the  
18       combined propagate signal for the five bits;

19       a first AND-NOR gate (212) having a first AND input  
20       receiving a propagate signal from the third bit, a second AND  
21       input receiving a generate signal from the second bit, a NOR  
22       input receiving a generate signal from the third bit and an  
23       output;

24       a second AND-NOR (213) gate having a first AND input  
25       receiving a propagate signal from the fifth bit, a second AND  
26       input receiving a generate signal from the fourth bit, a NOR  
27       input receiving a generate signal from the fifth bit and an  
28       output;

29       a second inverter (307) having an input receiving a generate  
30 signal from the first bit and an output;  
31       a OR-NAND gate (255) having a first OR input connected to  
32 said output of said first NAND gate, a second OR input connected  
33 to said output of said second inverter, a NAND input connected to  
34 said output of said first AND-NOR gate and an output;  
35       a third inverter (308) having an input connected to said  
36 output of said second NAND gate and an output;  
37       a fourth inverter (309) having an input connected to said  
38 output of said second AND-NOR gate and an output;  
39       a third AND-NOR (214) gate having a first AND input  
40 connected to said output of said OR-NAND gate, a second AND input  
41 connected to said output of said third inverter, a NOR input  
42 connected to said output of said fourth inverter and an output;  
43 and  
44       a fifth inverter (311) having an input connected to said  
45 output of said third AND-NOR gate and an output generating the  
46 combined generate signal for the five bits.

1       32. (New) The carry look ahead circuit of claim 31, wherein:  
2 said first, second and third AND-NOR gates include  
3       a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said first AND input,  
6       a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and a gate connected to said second AND  
9 input,  
10       a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and the  
12 output and a gate connected to said NOR input,

13           a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16           a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19           a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1       33. (New) The carry look ahead circuit of claim 31, wherein:  
2 said first, second and third AND-NOR gates include

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said NOR input,

6           a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and said output and a gate connected to  
9 said first AND input,

10          a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and said  
12 output and a gate connected to said second AND input,

13          a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16          a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19          a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1 34. (New) The carry look ahead circuit of claim 31, wherein:  
2 said OR-NAND gate includes

3 a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6 a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9 a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12 a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said OR input,

15 a second N-channel transistor having a source-drain  
16 path connected between said second intermediate node and  
17 ground and a gate connected to said first OR input, and

18 a third N-channel transistor having a source-drain path  
19 connected between said second intermediate node and ground  
20 and a gate connected to said second OR input.

1 35. (New) The carry look ahead circuit of claim 31, wherein:  
2 said OR-NAND gate includes

3 a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6 a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9 a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12           a first N-channel transistor having a source-drain path  
13       connected between said output and a second intermediate node  
14       and a gate connected to said first OR input,  
15           a second N-channel transistor having a source-drain  
16       path connected between said output and said second  
17       intermediate node and a gate connected to said second OR  
18       input, and  
19           a third N-channel transistor having a source-drain path  
20       connected between said second intermediate node and ground  
21       and a gate connected to said NAND input.

1       36. (New) A 6-bit carry look ahead circuit forming a  
2       combined propagate signal and a combined generated signal  
3       comprising:

4           a first NAND gate (120) having a first input receiving a  
5       propagate signal from the first bit, a second input receiving a  
6       propagate signal from the second bit and an output;

7           a second NAND gate (121) having a first input receiving a  
8       propagate signal from the third bit, a second input receiving a  
9       propagate signal from the fourth bit and an output;

10          a third NAND gate (122) having a first input receiving a  
11       propagate signal from the fifth bit, a second input receiving a  
12       propagate signal from the sixth bit and an output;

13          a NOR gate (123) having a first input connected to said  
14       output of said first NAND gate, a second input connected to said  
15       output of said second NAND gate and an output;

16          a first inverter (315) having an input connected to said  
17       output of said third NAND gate and an output;

18          a fourth NAND gate (124) having a first input connected to  
19       said output of said third NOR gate, a second input connected to  
20       said output of said first inverter and an output;

21        a second inverter (316) having an input connected to said  
22 output of said fourth NAND gate and an output generating the  
23 combined propagate signal for the six bits;

24        a first AND-NOR gate (215) having a first AND input  
25 receiving a generate signal from the first bit, a second AND  
26 input receiving a propagate signal from the second bit, a NOR  
27 input receiving a generate signal from the second bit and an  
28 output;

29        a second AND-NOR (216) gate having a first AND input  
30 receiving a propagate signal from the fourth bit, a second AND  
31 input receiving a generate signal from the third bit, a NOR input  
32 receiving a generate signal from the fourth bit and an output;

33        a first OR-NAND gate (256) having a first OR input connected  
34 to said output of said first AND-NOR gate, a second OR input  
35 connected to said output of said second NAND gate, a NAND input  
36 connected to said output of said second AND-NOR gate and an  
37 output;

38        a third inverter (312) having an input receiving a generate  
39 signal of the fifth bit and an output;

40        a fourth inverter (313) having an input connected receiving  
41 a propagate signal of the sixth bit and an output;

42        a fifth inverter (314) having an input receiving a generate  
43 signal of the sixth bit and an output;

44        a second OR-NOR gate (256) gate having a first OR input  
45 connected to said output of said third inverter, a second OR  
46 input connected to said output of said fourth inverter, a NAND  
47 input connected to said output of said fourth inverter and an  
48 output; and

49        a third AND-NOR gate (217) having a first AND input  
50 connected to said output of said first OR-NOR gate, a second AND  
51 input connected to said output of said second inverter, a NOR  
52 input and an output;

53       a sixth inverter (317) having an input connected to said  
54 output of said third AND-NOR gate and an output generating the  
55 combined generate signal for the six bits.

1       37. (New) The carry look ahead circuit of claim 36, wherein:  
2       said first, second and third AND-NOR gates include  
3       a first P-channel transistor having a source-drain path  
4       connected between a supply voltage and an first intermediate  
5       node and a gate connected to said first AND input,  
6       a second P-channel transistor having a source-drain  
7       path connected between a supply voltage and said first  
8       intermediate node and a gate connected to said second AND  
9       input,  
10       a third P-channel transistor having a source-drain path  
11       connected between said first intermediate node and the  
12       output and a gate connected to said NOR input,  
13       a first N-channel transistor having a source-drain path  
14       connected between said output and a second intermediate node  
15       and a gate connected to said first AND input,  
16       a second N-channel transistor having a source-drain  
17       path connected between said second intermediate node and  
18       ground and a gate connected to said second AND input, and  
19       a third N-channel transistor having a source-drain path  
20       connected between said output and ground and a gate  
21       connected to said NOR input.

1       38. (New) The carry look ahead circuit of claim 36, wherein:  
2       said first, second and third AND-NOR gates include  
3       a first P-channel transistor having a source-drain path  
4       connected between a supply voltage and an first intermediate  
5       node and a gate connected to said NOR input,

6           a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and said output and a gate connected to  
9 said first AND input,

10          a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and said  
12 output and a gate connected to said second AND input,

13          a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16          a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19          a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1       39. (New) The carry look ahead circuit of claim 36, wherein:  
2 said first and second OR-NAND gates include

3          a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6          a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9          a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12          a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said OR input,



15           a second N-channel transistor having a source-drain  
16 path connected between said second intermediate node and  
17 ground and a gate connected to said first OR input, and  
18           a third N-channel transistor having a source-drain path  
19 connected between said second intermediate node and ground  
20 and a gate connected to said second OR input.

1       40. (New) The carry look ahead circuit of claim 36, wherein:  
2 said first and second OR-NAND gate include  
3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,  
6           a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,  
9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,  
12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said first OR input,  
15           a second N-channel transistor having a source-drain  
16 path connected between said output and said second  
17 intermediate node and a gate connected to said second OR  
18 input, and  
19           a third N-channel transistor having a source-drain path  
20 connected between said second intermediate node and ground  
21 and a gate connected to said NAND input.

1       41. (New) A 6-bit carry look ahead circuit forming a  
2 combined propagate signal and a combined generated signal  
3 comprising:

4       a first NAND gate (125) having a first input receiving a  
5 propagate signal from the first bit, a second input receiving a  
6 propagate signal from the second bit and an output;  
7       a second NAND gate (126) having a first input receiving a  
8 propagate signal from the third bit, a second input receiving a  
9 propagate signal from the fourth bit and an output;  
10       a third NAND gate (127) having a first input receiving a  
11 propagate signal from the fifth bit, a second input receiving a  
12 propagate signal from the sixth bit and an output;  
13       a first NOR gate (128) having a first input connected to  
14 said output of said second NAND gate, a second input connected to  
15 said output of said third NAND gate and an output;  
16       a first inverter (319) having an input connected to said  
17 output of said first NOR gate and an output;  
18       a second NOR gate (129) having a first input connected to  
19 said output of said first NAND gate, a second input connected to  
20 said output of said first inverter and an output generating the  
21 combined propagate signal for the six bits;  
22       a first AND-NOR gate (218) having a first AND input  
23 receiving a propagate signal from the second bit, a second AND  
24 input receiving a generate signal from the first bit, a NOR input  
25 receiving a generate signal from the second bit and an output;  
26       a second inverter (318) having an input connected to said  
27 output of said first AND-NOR gate and an output;  
28       a second AND-NOR (219) gate having a first AND input  
29 receiving a propagate signal from the fourth bit, a second AND  
30 input receiving a generate signal from the third bit, a NOR input  
31 receiving a generate signal from the fourth bit and an output;  
32       a third AND-NOR (220) gate having a first AND input  
33 receiving a propagate signal from the sixth bit, a second AND  
34 input receiving a generate signal from the fifth bit, a NOR input  
35 receiving a generate signal from the sixth bit and an output;

36       a OR-NAND gate (258) having a first OR input connected to  
37 said output of said second AND-NOR gate, a second OR input  
38 connected to said output of said third NAND gate, a NAND input  
39 connected to said output of said third AND-NOR gate and an  
40 output;  
41       a fourth AND-NOR gate (221) having a first AND input  
42 connected to said output of said first OR-NOR gate, a second AND  
43 input connected to said output of said first NOR gate, a NOR  
44 input and an output; and  
45       a third inverter (320) having an input connected to said  
46 output of said fourth AND-NOR gate and an output generating the  
47 combined generate signal for the six bits.

1       42. (New) The carry look ahead circuit of claim 41, wherein:  
2       said first, second, third and fourth AND-NOR gates include  
3       a first P-channel transistor having a source-drain path  
4       connected between a supply voltage and an first intermediate  
5       node and a gate connected to said first AND input,  
6       a second P-channel transistor having a source-drain  
7       path connected between a supply voltage and said first  
8       intermediate node and a gate connected to said second AND  
9       input,  
10       a third P-channel transistor having a source-drain path  
11       connected between said first intermediate node and the  
12       output and a gate connected to said NOR input,  
13       a first N-channel transistor having a source-drain path  
14       connected between said output and a second intermediate node  
15       and a gate connected to said first AND input,  
16       a second N-channel transistor having a source-drain  
17       path connected between said second intermediate node and  
18       ground and a gate connected to said second AND input, and

19           a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1       43. (New) The carry look ahead circuit of claim 41, wherein:  
2 said first, second, third and fourth AND-NOR gates include

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said NOR input,

6           a second P-channel transistor having a source-drain  
7 path connected between a supply voltage and said first  
8 intermediate node and said output and a gate connected to  
9 said first AND input,

10          a third P-channel transistor having a source-drain path  
11 connected between said first intermediate node and said  
12 output and a gate connected to said second AND input,

13          a first N-channel transistor having a source-drain path  
14 connected between said output and a second intermediate node  
15 and a gate connected to said first AND input,

16          a second N-channel transistor having a source-drain  
17 path connected between said second intermediate node and  
18 ground and a gate connected to said second AND input, and

19          a third N-channel transistor having a source-drain path  
20 connected between said output and ground and a gate  
21 connected to said NOR input.

1       44. (New) The carry look ahead circuit of claim 41, wherein:  
2 said OR-NAND gate includes

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6           a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said OR input,

15           a second N-channel transistor having a source-drain  
16 path connected between said second intermediate node and  
17 ground and a gate connected to said first OR input, and

18           a third N-channel transistor having a source-drain path  
19 connected between said second intermediate node and ground  
20 and a gate connected to said second OR input.

1       45. (New) The carry look ahead circuit of claim 41, wherein:  
2 said OR-NAND gate includes

3           a first P-channel transistor having a source-drain path  
4 connected between a supply voltage and an first intermediate  
5 node and a gate connected to said second OR input,

6           a second P-channel transistor having a source-drain  
7 path connected between said first intermediate node and said  
8 output and a gate connected to said first OR input,

9           a third P-channel transistor having a source-drain path  
10 connected between the supply voltage and said output and a  
11 gate connected to said NAND input,

12           a first N-channel transistor having a source-drain path  
13 connected between said output and a second intermediate node  
14 and a gate connected to said first OR input,

15           a second N-channel transistor having a source-drain  
16 path connected between said output and said second

17 intermediate node and a gate connected to said second OR  
18 input, and  
19 a third N-channel transistor having a source-drain path  
20 connected between said second intermediate node and ground  
21 and a gate connected to said NAND input.